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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,827	11/04/2003	Kazuhisa Sakihama	244844US2S	5577

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EXAMINER	
KITOV, ZEEV	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Supplemental Notice of Allowability	Application No. 10/699,827	Applicant(s) SAKIHAMA ET AL.	
	Examiner Zeev Kitov	Art Unit 2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *09/30/05*.

2. ☒ The allowed claim(s) is/are *1 - 5, 7 - 9, 11, 12, 14 - 18*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 09/30/05
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

REASONS FOR ALLOWANCE

Examiner acknowledges a submission of the IDS including the Japanese Patent Office Action filed on September 30, 2005.

The following is an examiner's statement of reasons for allowance:

An amended independent Claim 1 discloses, inter alia, a clamp circuit connected to the first pad and the second pad, and a control circuit, which renders the clamp circuit conducting when the same potential as applied to the second pad is applied to the third pad before the semiconductor integrated circuit is incorporated into an end product, and to render the clamp circuit non-conducting when a predetermined potential is applied to the third pad after the semiconductor integrated circuit is incorporated into the end product.

The closest reference for the claim is Ma, which discloses some elements of the claim, such as: the control circuit is configured to render the clamp circuit conducting when the same potential as applied to the second pad is applied to the third pad before the semiconductor integrated circuit is incorporated into an end product and to render the clamp circuit non-conducting when a predetermined potential is applied to the third pad after the semiconductor integrated circuit is incorporated into the end product. It further discloses the first pad and the second pad coupled in accordance with the claim. However, while the claim language states: "a clamp circuit connected to the first pad and the second pad", the reference discloses the clamp circuit connected between the

first pad and the second pad. Additionally, the clamp of the reference can not be considered as permanently connected to the second pad (Vcc terminal), due to a presence of since some active parts between the clamp and the terminal, such as switching transistor 22 in Fig. 5, which makes the connection conditional on its state.

Another close reference is Chittipeddi et al. (US 6,556,409), which discloses the second pad (the ground pad), while the first pad may be inherent in the structure, as the power supply pad Vcc. It further discloses the third pad (JTAG interface, col. 5, lines 34 – 47). Before incorporation of the reference circuit into the end product, when the same potential as applied to the second pad (zero potential of the ground), the circuit can be activated when ESD event occurs, since for activation of the clamp, or "to "render the clamp conductive" (clamp is the element 213 in Fig. 2A) the ESD potential or some other external overstress potential should be additionally applied. After incorporation into thee end product, the circuit is not conductive. This way of functioning is different from Claim 1 of the Application, wherein the control signal plays an active role in the rendering the clamp either conductive or non-conductive. According to American Heritage Dictionary, the word "rendering" stands for "to direct the execution of". Therefore, the control signal rendering the clamp either conductive (without necessity for an external additional signal) before incorporation into the final product, or non-conductive after incorporation into the final product of Claim 1 is different from the way of functioning of the reference circuit.

The Japanese Office Action recites JP 2002-049293 and JP 08-097376 as prior art sufficient for rejection of the only independent Claim 1. Both references have been

analyzed. Both references disclose circuits satisfying some of Claim 1 limitations, such as: a first pad which is used as an external connection terminal to be connected to a semiconductor integrated circuit; a second pad which is used as an external connection terminal to be connected to the semiconductor integrated circuit; a clamp circuit connected to the first pad and the second pad; a control circuit which is configured to control the clamp circuit; and a third pad connected to the control circuit, wherein the control circuit is configured to render the clamp circuit conducting when the same potential as applied to the second pad is applied to the third pad and render the clamp circuit non-conducting when a predetermined potential is applied to the third pad.

However, none of the references satisfies the following claim limitation: a control circuit which is configured to control the clamp circuit; and a third pad connected to the control circuit, wherein the control circuit is configured to render the clamp circuit conducting when the same potential as applied to the second pad is applied to the third pad before the semiconductor integrated circuit is incorporated into an end product and render the clamp circuit non-conducting when a predetermined potential is applied to the third pad after the semiconductor integrated circuit is incorporated into the end product. The underlined text shows the limitation not disclosed in any of the references. These functional limitations are supported by the structure and process disclosed in Specification. The Drawings show in Fig. 13 and 14 the circuit capable of programming the integrated circuit to change its threshold when the circuit is incorporated into the end product. These programming features are disclosed by Specification (page 29, line 16 –

page 33, line 2). None of the references recite such limitations. Their disclosures do not include a structure or process capable of such programming.

Since the Claim 1 is the only independent Claim, the Application is in condition for Allowance.

Allowability resides, at least in part, in the above-described limitations, which has not been disclosed in the Prior Art in a search.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose telephone number is (571) 272-2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is 571–273–8300 for all communications.

Z.K.
07/07/2005

BRIAN SIRCUS
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